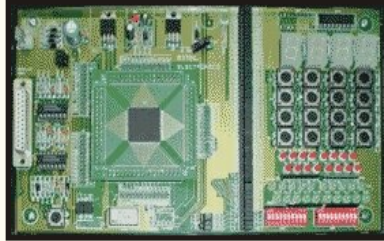




VLSI DESIGN TRAINER

MODEL VLSI100G

This trainer has been designed with a view to provide practical and experimental Knowledge of VLSI Design technique on a P.C.B.



Features

Xilinx Devices

Spartan-3AN (XC3S700AN-FG484)
Platform Flash (XCF04S-VOG20C)

Clocks

50 MHz crystal oscillator on-board
Open slot for optional user-installed clock

Memory

4 Mbit Platform Flash PROM
32M x 16 DDR2 SDRAM
32 Mbit parallel Flash
2-16 Mbit SPI Flash devices

Analog Interface Devices

4-channel D/A converter
2-channel A/D converter
Signal amplifier

Connectors and Interfaces

Ethernet 10/100 PHY
JTAG USB download port
Two 9-pin RS-232 serial port
PS/2-style mouse/keyboard port
15-pin VGA connector capable of 4,096 colors
One FX2 100-pin and two 6-pin expansion connectors
20 user I/O available on standard header pins
Stereo mini-jack for PWM audio
Rotary/push button function switch
Eight individual LED outputs
Four slider switches, four push-button switches.

In keeping view of SIGMA policy of continuous development and improvement, the Specifications may be changed without prior notice or obligation.

Sigma Trainers and Kits
E-113, Jai Ambe Nagar,
Near Udgam School,
Thaltej,
AHMEDABAD - 380054.
INDIA.

Phone(O): +91-79-26852427/ 26850829
Phone(F): +91-79-26767512/ 26767648
Fax : +91-79-26840290/ 26840290
Mobile : +91-9824001168
Email : sales@sigmatrainers.com
: sigmatrainers@sify.com
Web : www.sigmatrainers.com

Dealer:-

EXPERIMRNTS

- 1 Introduction to VHDL
- 2 To study VHDL entities and coding styles
- 3 To study signals and data types
- 4 To implement various basic logic gates using VHDL
- 5 To implement universal logic gates using VHDL
- 6 To implement different Flip-Flop using VHDL
- 7 To implement Multiplexer using VHDL
- 8 To implement decoder/Encoder using VHDL
- 9 To implement 4 bit adder/subtractor using VHDL
- 10 To implement 4 bit adder for carry look ahead concept
- 11 To implement 4 bit universal counter, up/down counter, asynchronous counter