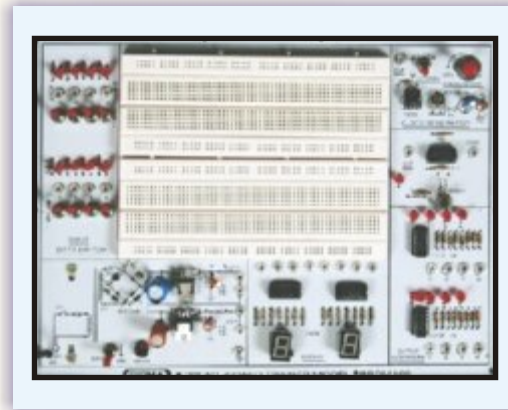




DIGITAL LAB TRAINER

MODEL BBDM100S

This trainer has been designed with a view to verify truth table of logic gates and address and to construct small digital circuits and perform various experiments.



SPECIFICATIONS

1. Breadboard : 172.5 mm x 128.5mm
Tie points : 1685
2. DC power supply : +5V-1A, 5V 500mA, +3V-15V
500mA (variable), -3V-15V, 500 mA (variable)
3. Pulse Generator
Frequency range : 1 Hz to 1 MH in 6 steps. Variable in between
Amplitude : 3V-15V (CMOS), 5V (TTL)
Duty cycle : 50%, TTL/CMOS output
4. Pulsers Switches : 2 nos. (Push to On)
5. Data switches : 8 nos. (Toggle switches for both TTL & CMOS)
7. LED Display : 8 nos. (TTL/CMOS Mode)
8. Seven Segment Display: 3 Nos.
9. Logic Probe : Logic level indicator for TTL/CMOS
10. Power : 220V \pm 10%, 50/60 Hz
11. Power Consumption : 3VA (approx.)
12. Accessories included : Mains cord, Operating and experimental Manual (with more than 20 designed Experiments), patch cords

In keeping view of SIGMA policy of continuous development and improvement, the Specifications may be changed without prior notice or obligation.

Sigma Trainers
E-103, Jai Ambe Nagar,
Near Udgam School, Thaltej,
AHMEDABAD - 380054.

Phone : 079-26852427 / 26767512
Fax : 079-26840290 / 26759661
ISDN : 079-26859162 / 26853758
Email : sales@sigmatrainers.com
: sigmatrainers@sify.com
Web : www.sigmatrainers.com

Dealer:-

Ready to use experimental Board

- a) Logic Gates
- b) Universal Gate NAND/NOR Gate
- c) EX-OR Gate implementation
- d) Demorgan's Theorem
- e) EX-OR Gate Application
- f) Code conversion (Binary to Gray and Gray to Binary code)
- g) Code conversion (BCD to excess-3 codes)
- h) Binary Adder/Subtractor
- i) Encoder/Decoder (8 to 3 line Encoder, 3 to 8 line Decoder)
- j) Multiplexer/Demultiplexer (4-1 line Multiplexer 1-4 line Demultiplexer)
- k) Flip-Flops (R-S, D,J-K,T Flip-Flops)
- l) Shift register 4 Bit serial in- parallel Out
- m) 4 Bit synchronous Binary counter (Up counter)
- n) 4 Bit Binary Ripple Counter (Up down Counter)
- o) BCD to 7 segment decoder
- p) Digital to Analog Converter (R-2R Ladder)